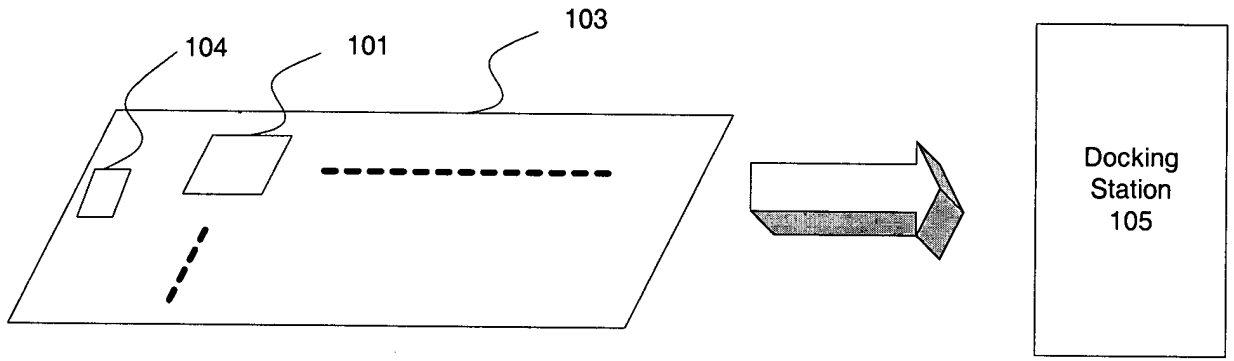

Figure 1A

100

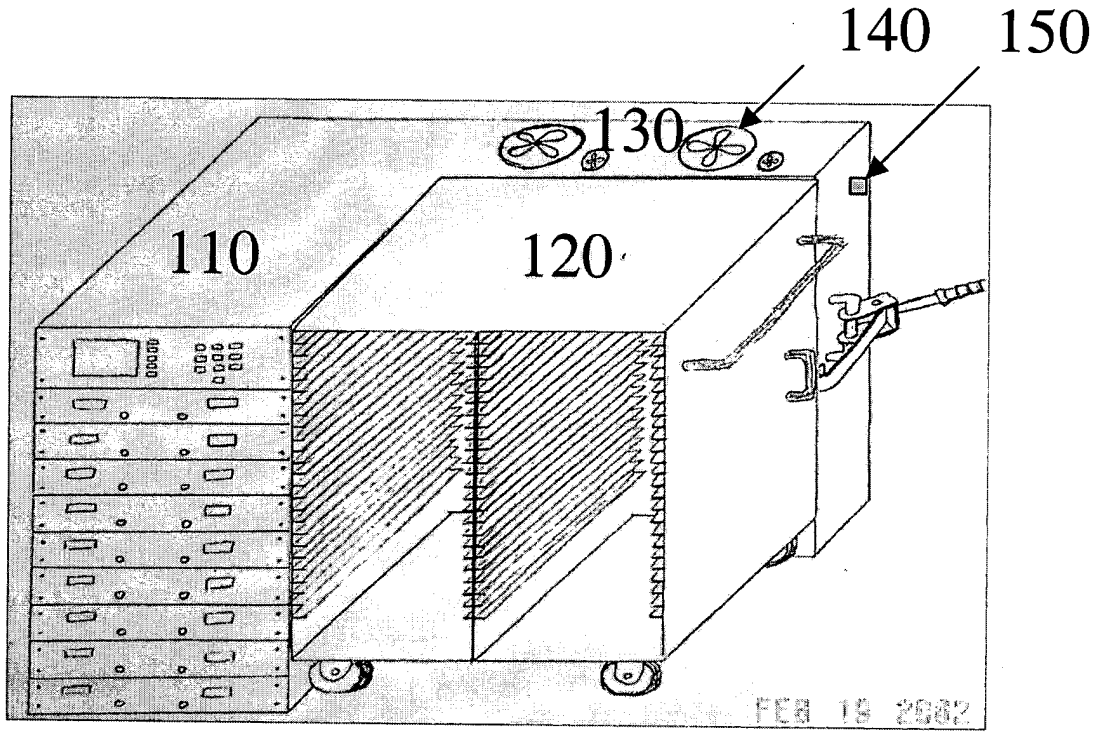

Figure 1B

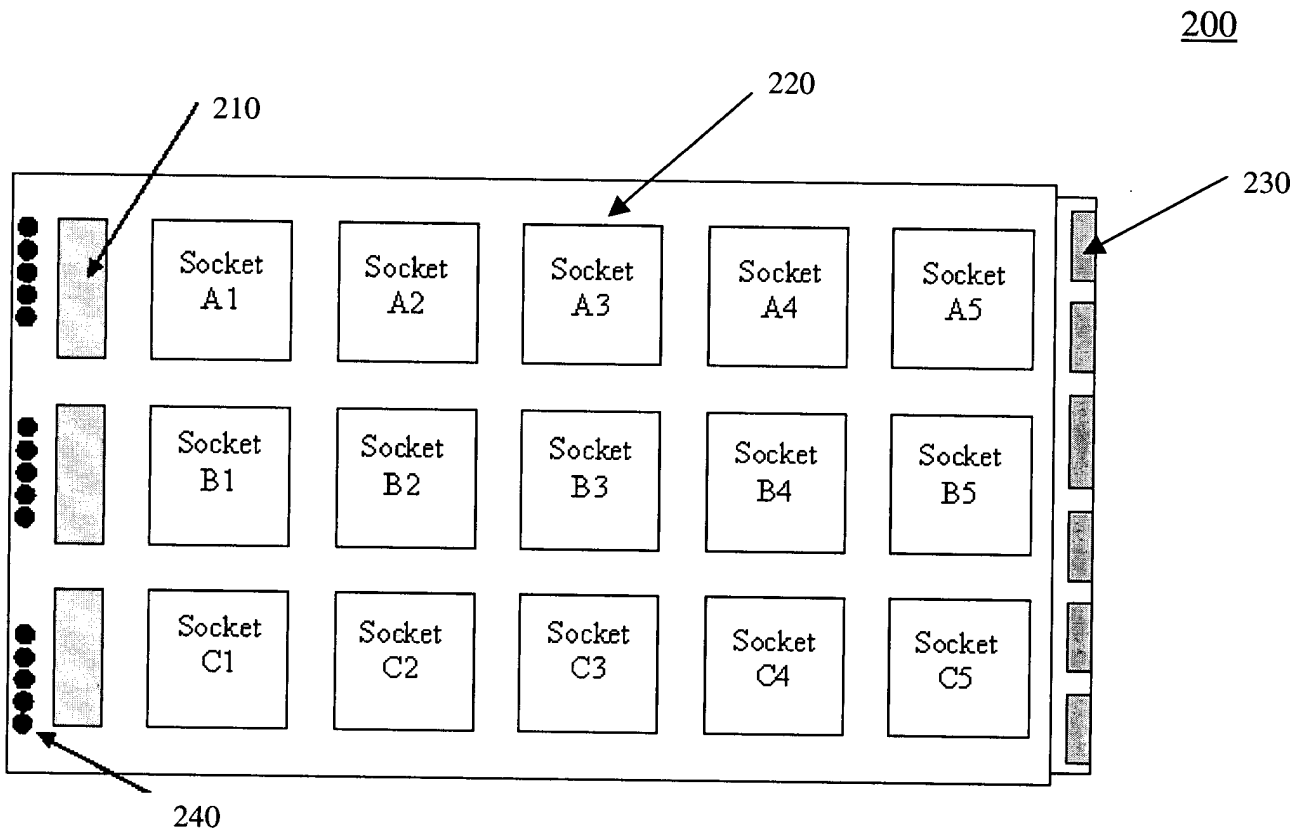
200
210
220
230
Socket A1
Socket A2
Socket A3
Socket A4
Socket A5
Socket B1
Socket B2
Socket B3
Socket B4
Socket B5
Socket C1
Socket C2
Socket C3
Socket C4
Socket C5
240

Figure 2

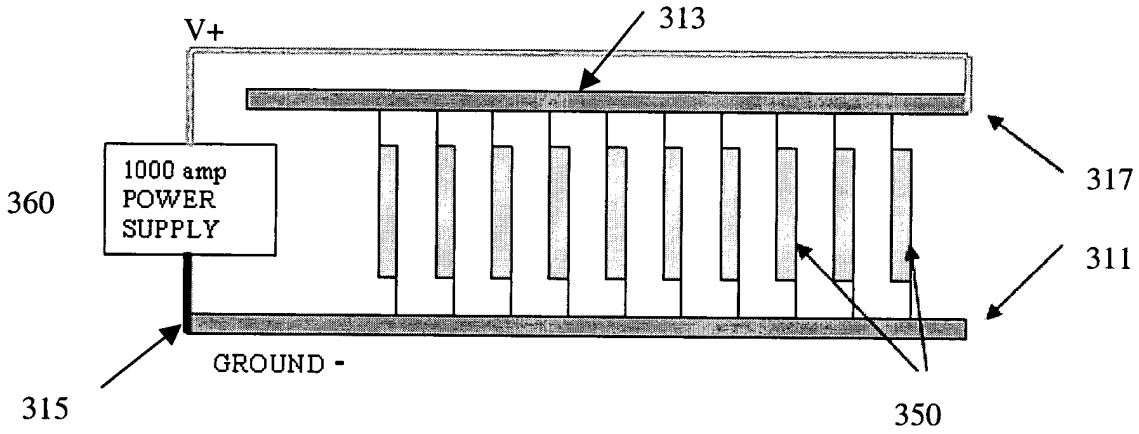

Figure 3

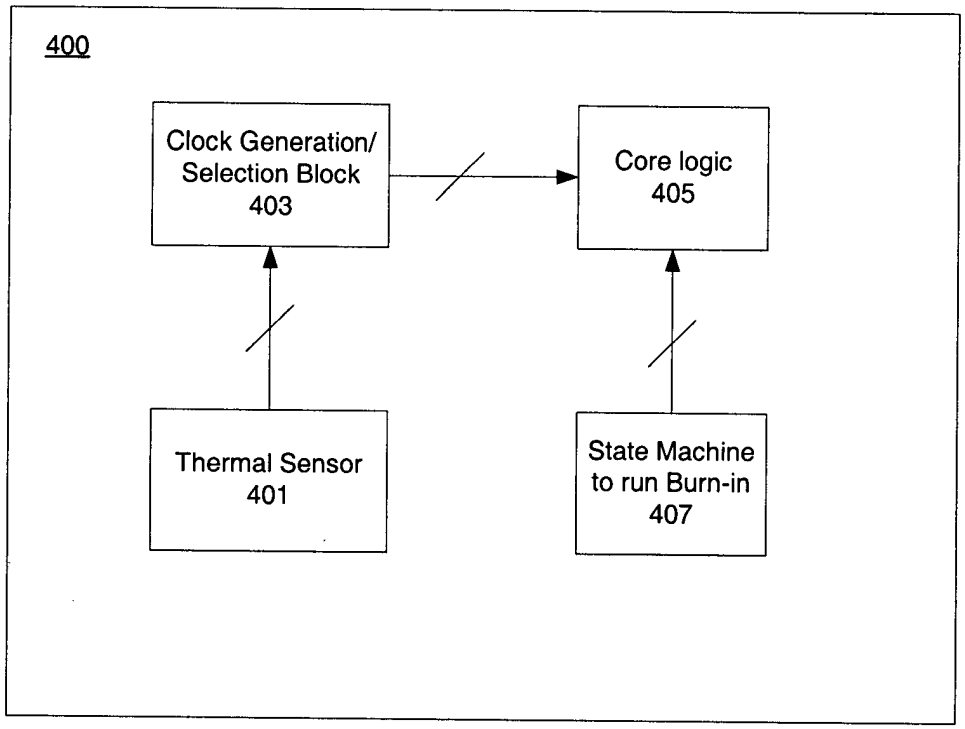
400
Clock Generation/
Selection Block
403
Core logic
405
Thermal Sensor
401
State Machine
to run Burn-in
407

Figure 4A

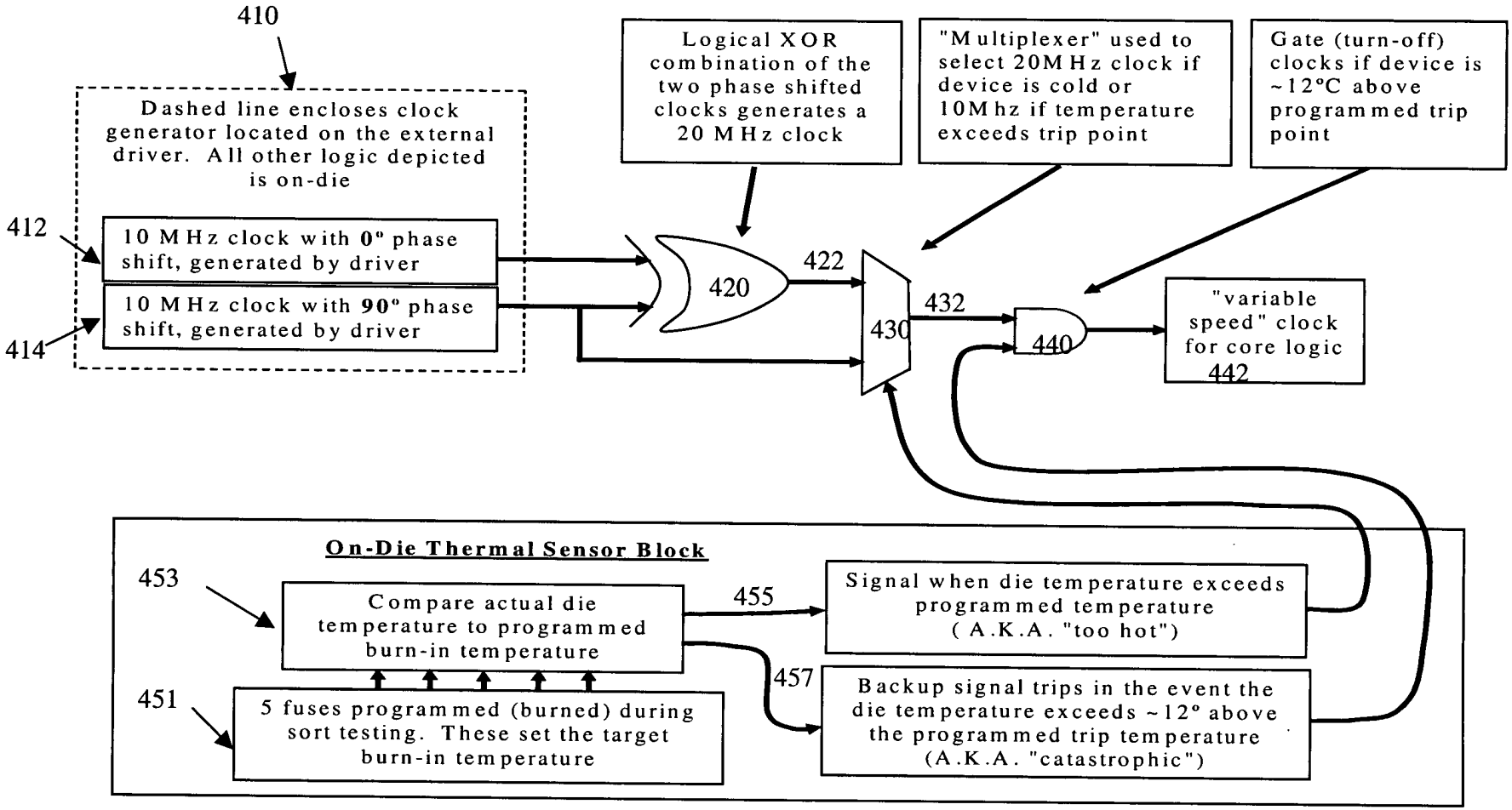
410
Dashed line encloses clock generator located on the external driver. All other logic depicted is on-die
412
10 MHz clock with 0° phase shift, generated by driver
414
10 MHz clock with 90° phase shift, generated by driver
Logical XOR combination of the two phase shifted clocks generates a 20 MHz clock
"Multiplexer" used to select 20MHz clock if device is cold or 10Mhz if temperature exceeds trip point
Gate (turn-off) clocks if device is ~12°C above programmed trip point
420
422
430
432
440
"variable speed" clock for core logic
442
On-Die Thermal Sensor Block
453
Compare actual die temperature to programmed burn-in temperature
455
Signal when die temperature exceeds programmed temperature (A.K.A. "too hot")
457
Backup signal trips in the event the die temperature exceeds ~12° above the programmed trip temperature (A.K.A. "catastrophic")
451
5 fuses programmed (burned) during sort testing. These set the target burn-in temperature

Figure 4B

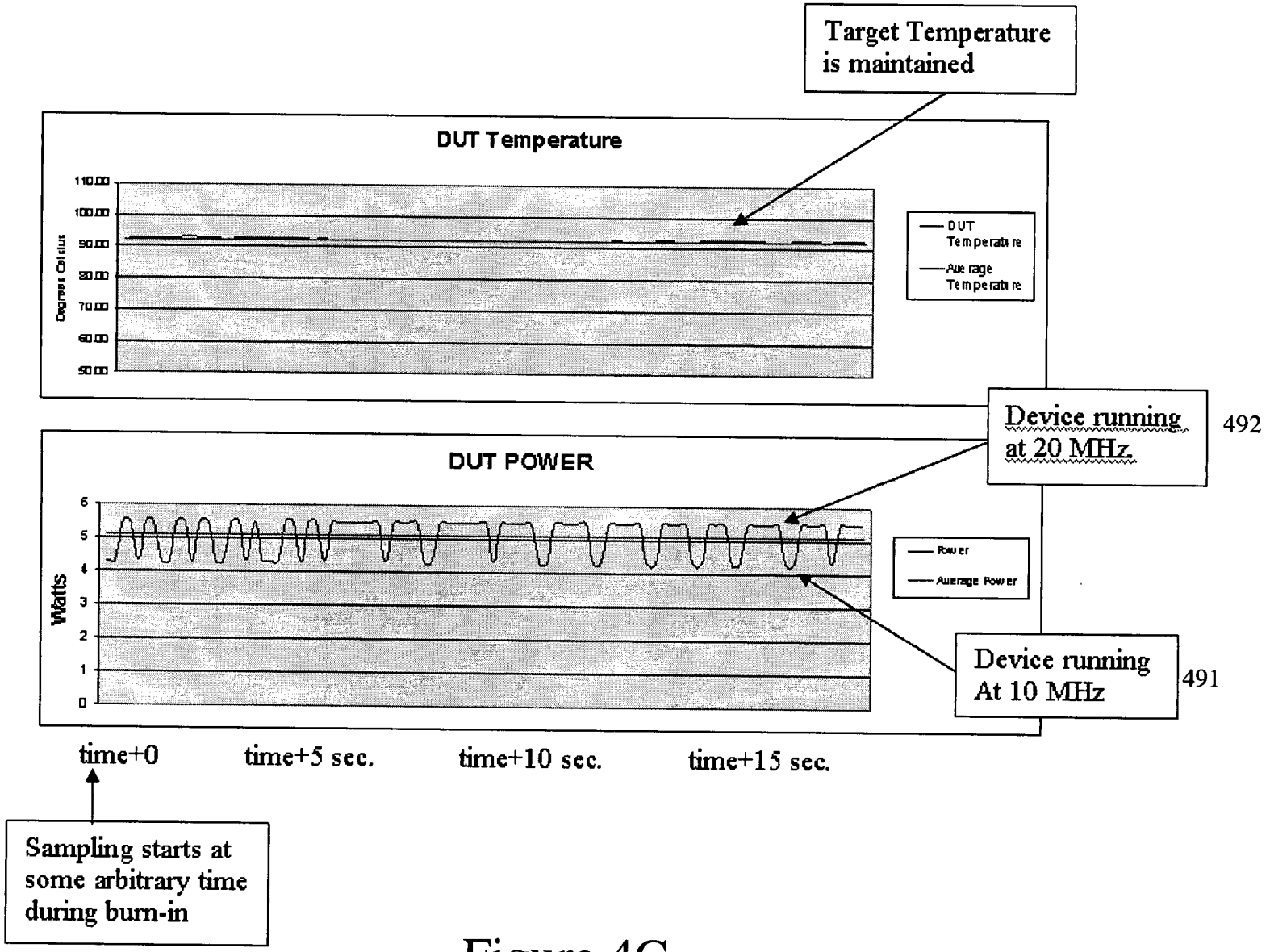
Target Temperature is maintained
DUT Temperature
110.00
100.00
90.00
80.00
70.00
60.00
50.00
Degrees Celsius
DUT Temperature
Average Temperature
Device running at 20 MHz.
492
DUT POWER
6
5
4
3
2
1
0
Watts
Power
Average Power
Device running At 10 MHz
491
time+0
time+5 sec.
time+10 sec.
time+15 sec.
Sampling starts at some arbitrary time during burn-in

Figure 4C

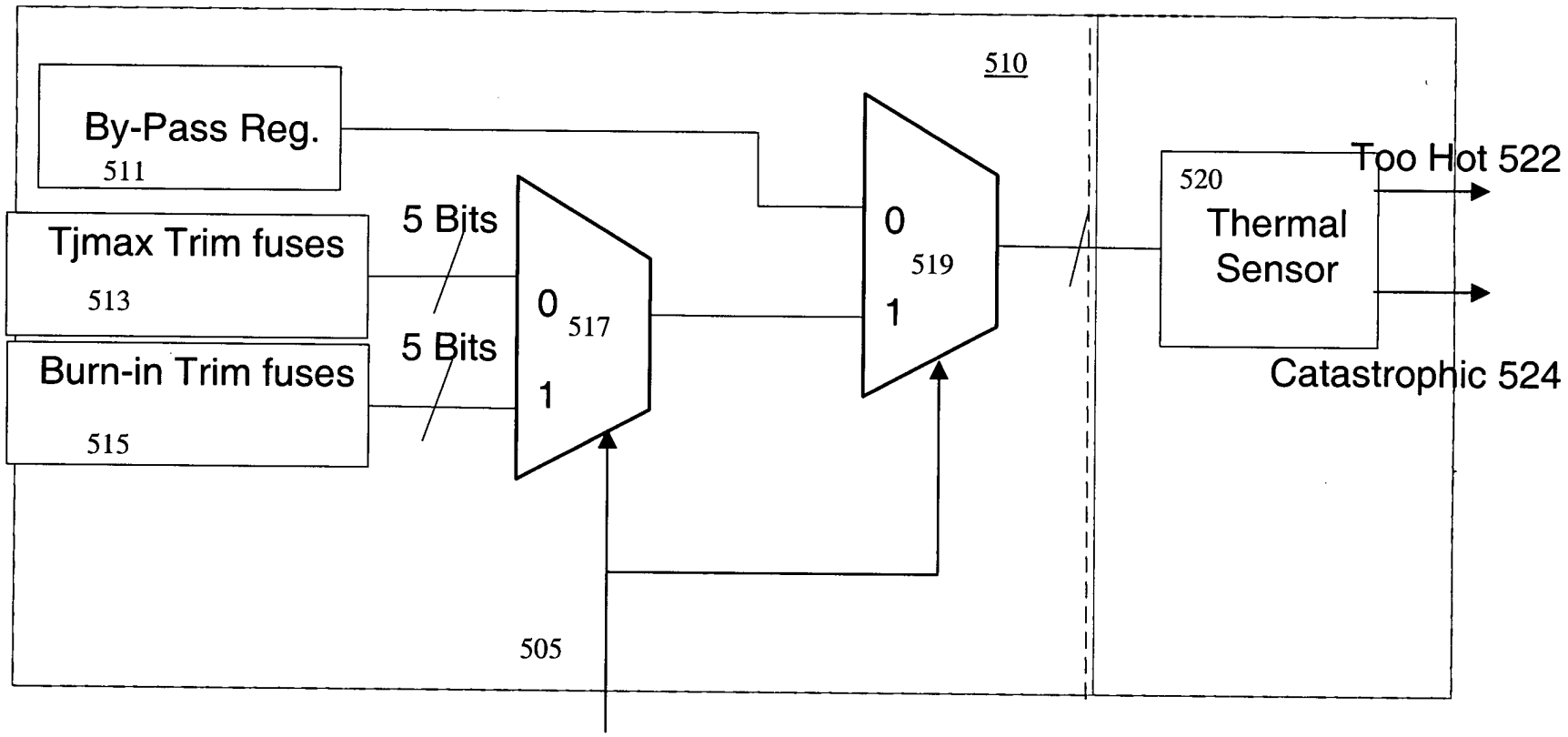
510
By-Pass Reg.
511
Tjmax Trim fuses
513
Burn-in Trim fuses
515
5 Bits
5 Bits
0
517
1
0
519
1
520
Thermal
Sensor
Too Hot 522
Catastrophic 524
505

Figure 5

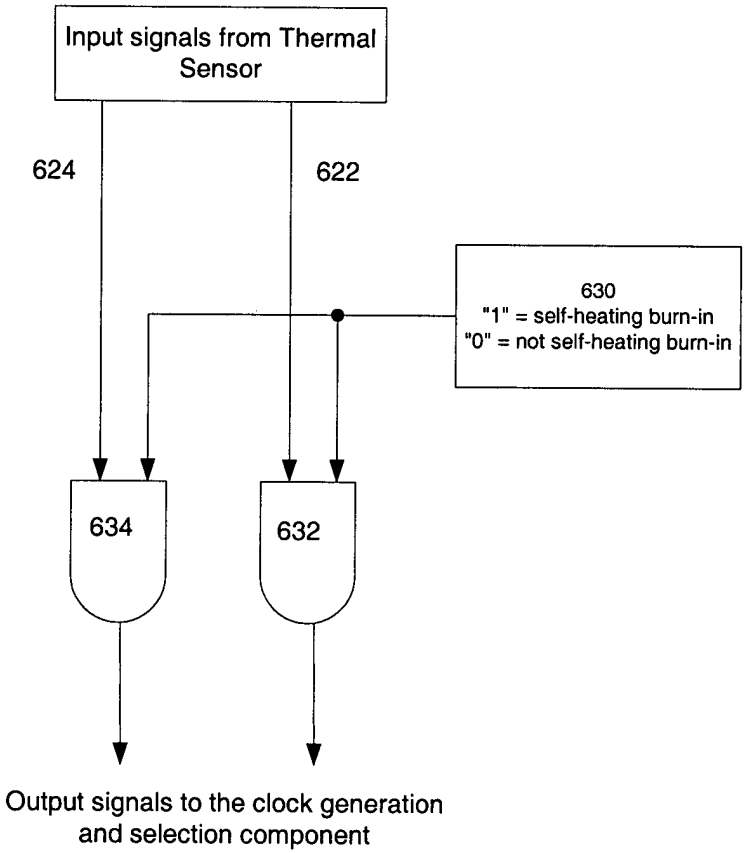
Input signals from Thermal Sensor
624
622
630
"1" = self-heating burn-in
"0" = not self-heating burn-in
634
632
Output signals to the clock generation and selection component

Figure 6

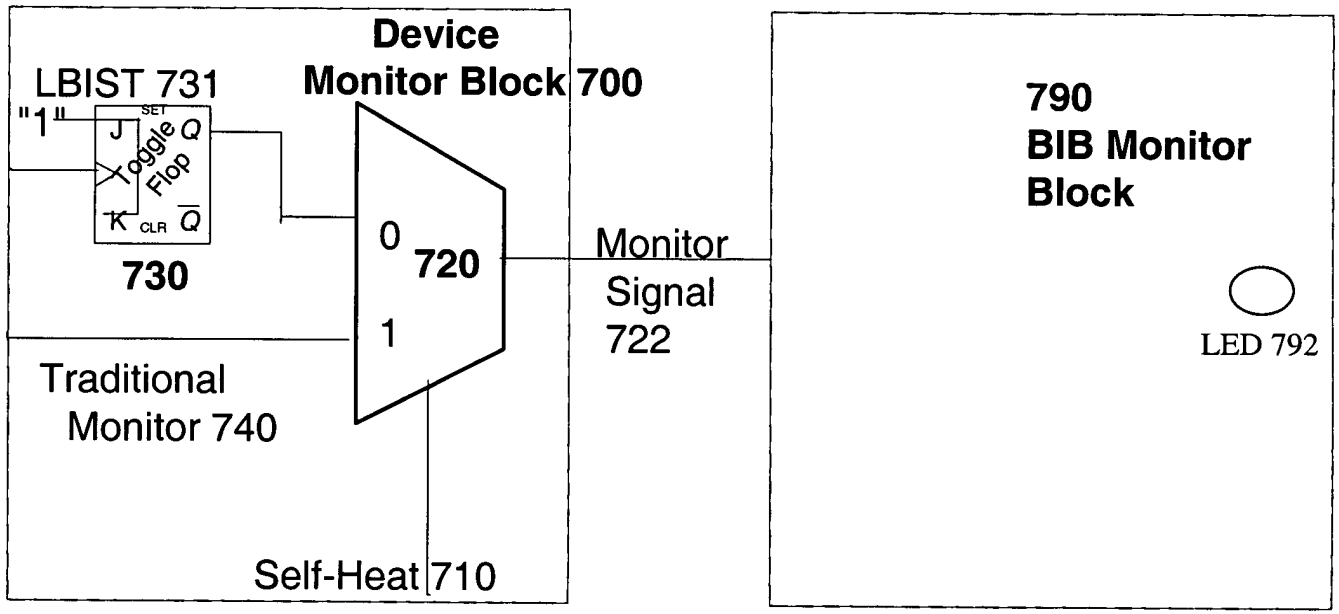
Device
Monitor Block 700
LBIST 731
"1"
SET
J
Toggle Flop
Q
K
CLR
Q
730
0
720
1
Traditional
Monitor 740
Monitor
Signal
722
Self-Heat 710
790
BIB Monitor
Block
LED 792

Figure 7

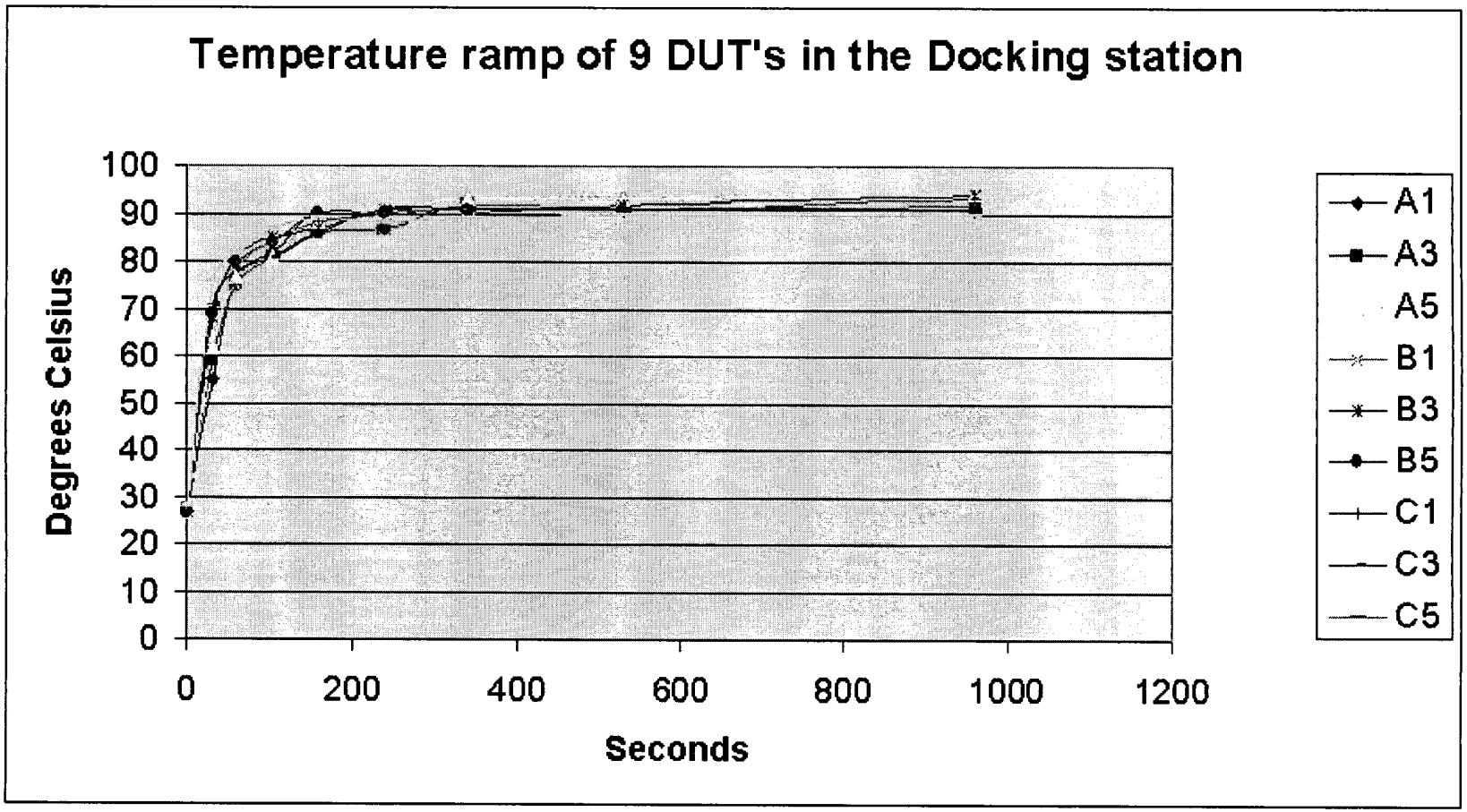
Temperature ramp of 9 DUT's in the Docking station
Degrees Celsius
100
90
80
70
60
50
40
30
20
10
0
0
200
400
600
800
1000
1200
Seconds
A1
A3
A5
B1
B3
B5
C1
C3
C5

Figure 8A

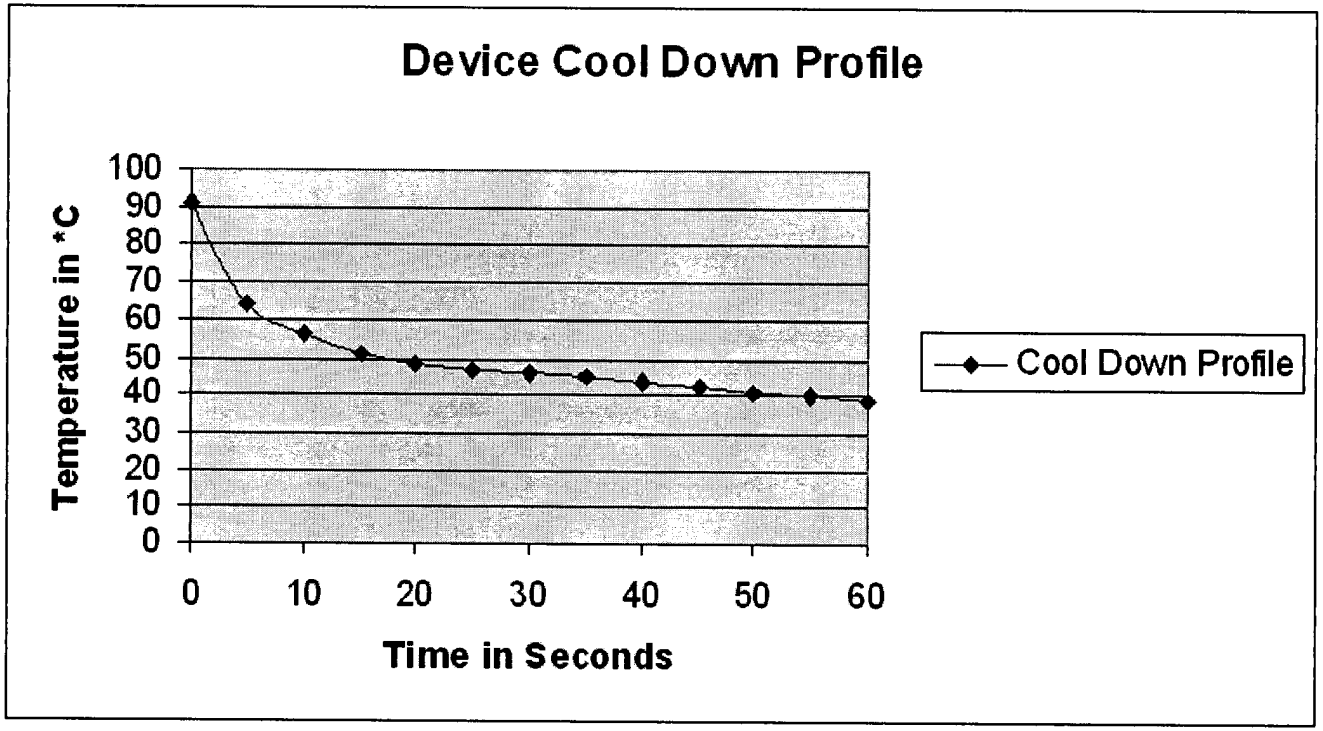
Device Cool Down Profile
Temperature in *C
100
90
80
70
60
50
40
30
20
10
0
0
10
20
30
40
50
60
Time in Seconds
Cool Down Profile

Figure 8B

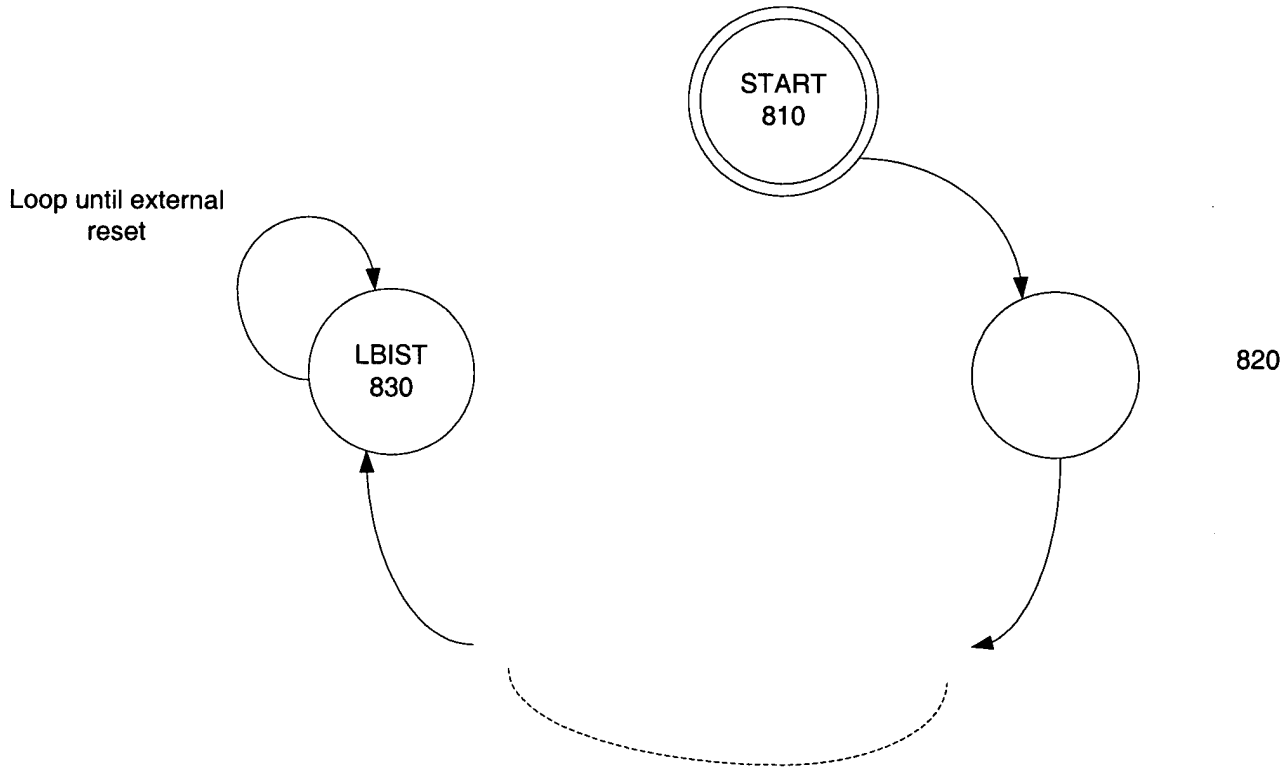

Figure 8C

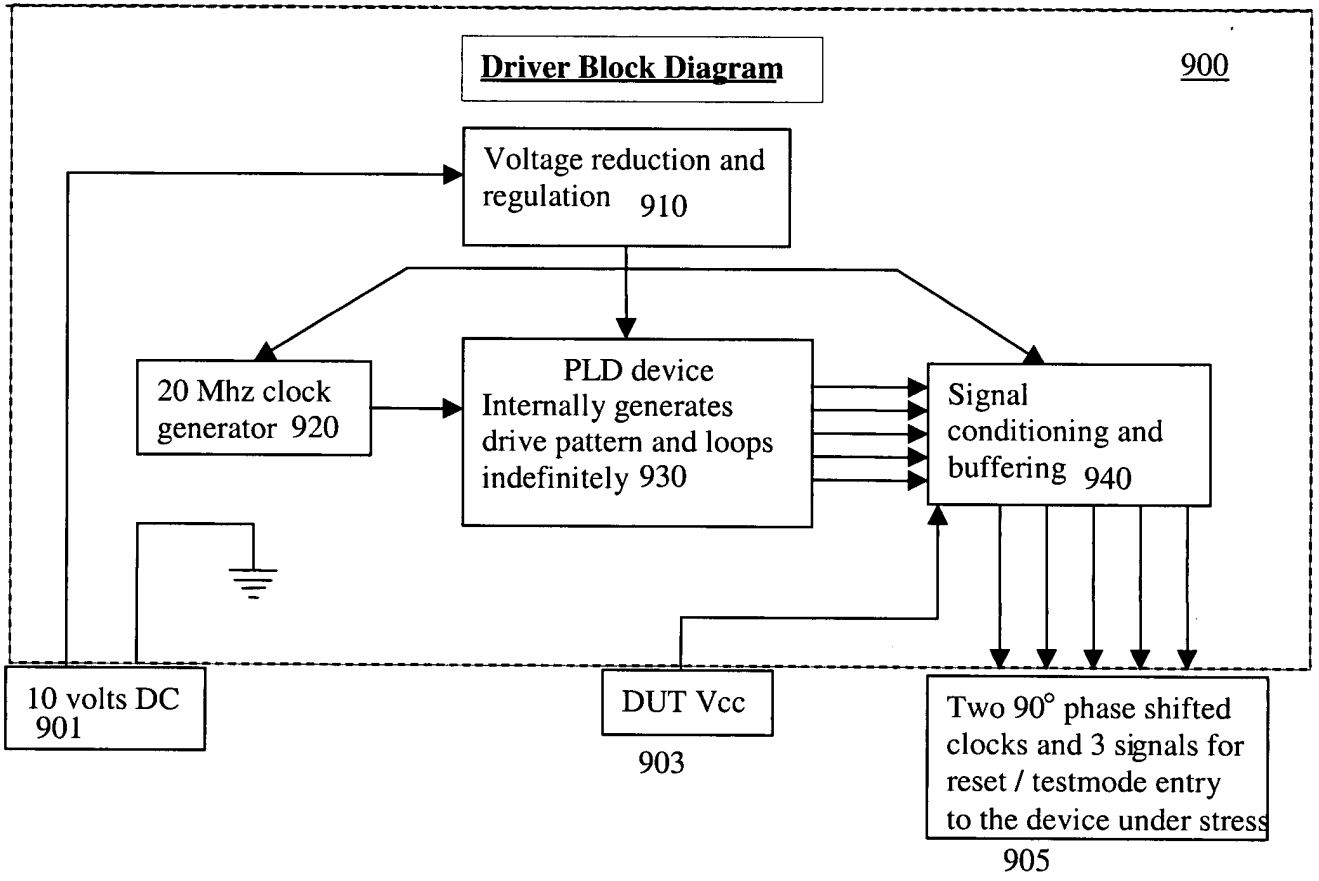
Driver Block Diagram
900
Voltage reduction and regulation 910
20 Mhz clock generator 920
PLD device Internally generates drive pattern and loops indefinitely 930
Signal conditioning and buffering 940
10 volts DC 901
DUT Vcc 903
Two 90° phase shifted clocks and 3 signals for reset / testmode entry to the device under stress 905

Figure 9

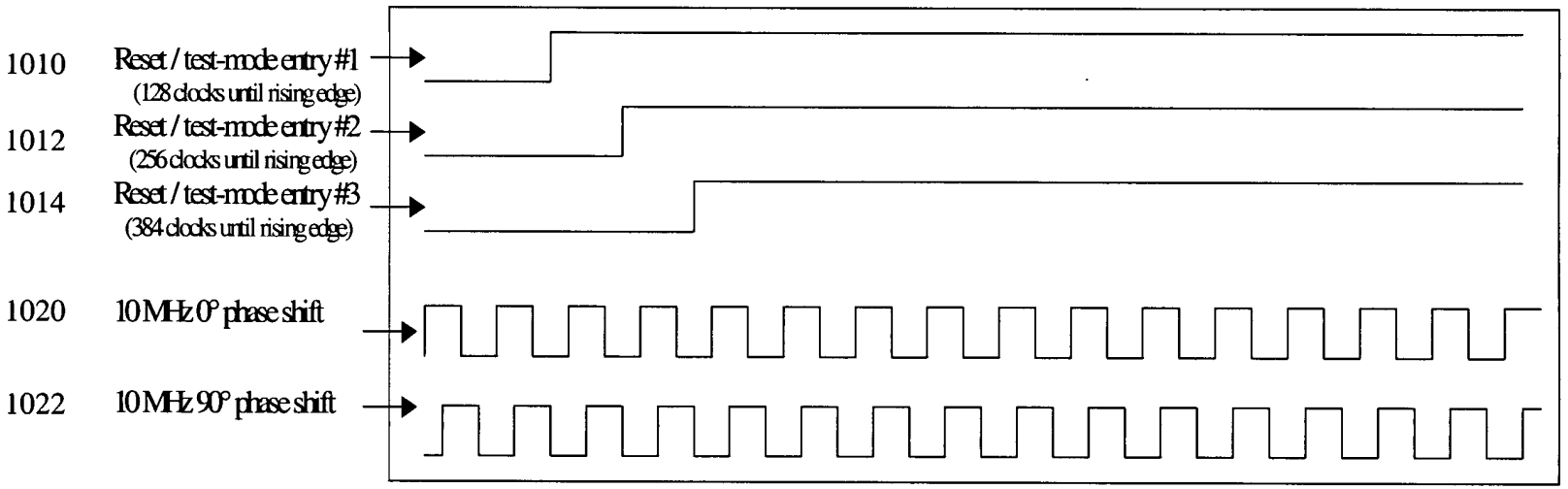
1010
Reset / test-mode entry #1
(128 clocks until rising edge)
1012
Reset / test-mode entry #2
(256 clocks until rising edge)
1014
Reset / test-mode entry #3
(384 clocks until rising edge)
1020
10 MHz 0° phase shift
1022
10 MHz 90° phase shift

Figure 10

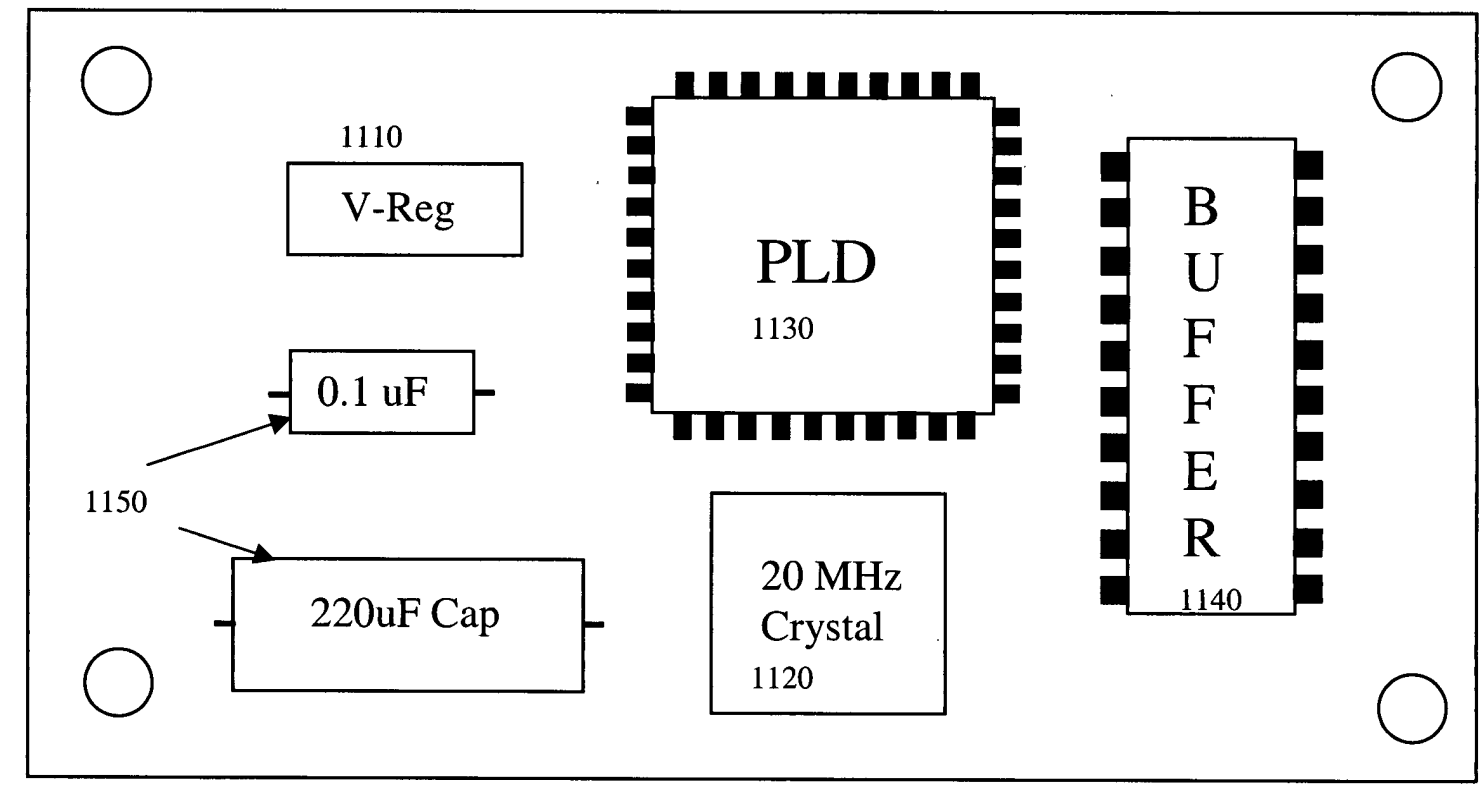
1100
1110
V-Reg
PLD
1130
B
U
F
F
E
R
1140
0.1 uF
1150
220uF Cap
20 MHz
Crystal
1120

Figure 11

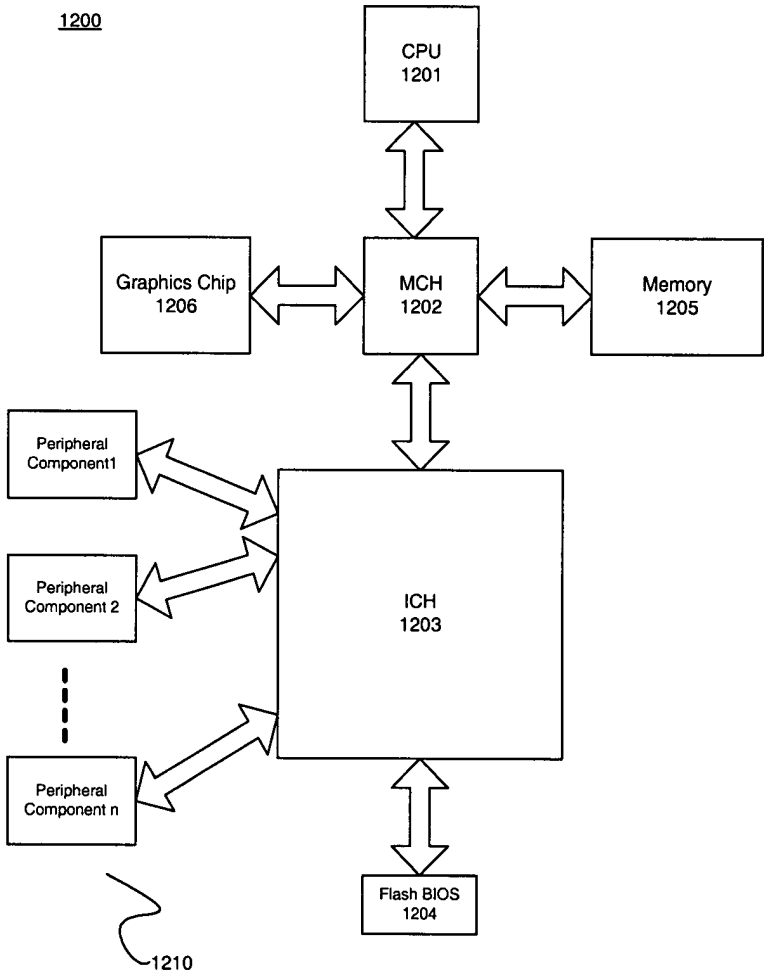
1200
CPU
1201
Graphics Chip
1206
MCH
1202
Memory
1205
Peripheral
Component1
Peripheral
Component 2
Peripheral
Component n
ICH
1203
Flash BIOS
1204
1210

Figure 12